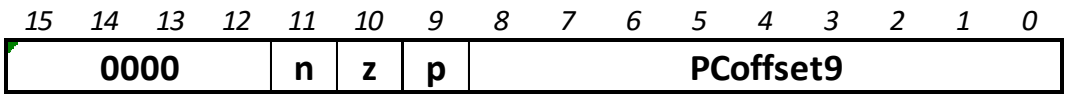
BR (0000) Instruction Cycle



Instruction Fetch

MAR ← PC

PC ← PC + 1

MDR ← memory[MAR]

IR ← MDR

Decode

IR[15:12] decoded

Evaluate Address

n/a

Operand Fetch

n/a

Execute

PC ← (IR[11] and N) or (IR[10] and Z) or (IR[9] and P) ?

PC + sign_ext$_{16}$(IR[8:0]) : PC

Store Result

n/a